2.4 GHz RF SoC FOR WIRELESS DIGITAL AUDIO STREAMING CC8520 - PurePath™ Wireless

APPLICATIONS

- **Wireless high-quality digital audio**
- **Wireless point-to-point audio link**
- **Wireless headphones**
- **Wireless loudspeakers**

FEATURES

Built-in audio protocol

- **CD-quality uncompressed audio**
- **Excellent robustness and co-existence through multiple techniques**
  - **Adaptive Frequency Hopping**
  - **Forward Error Correction**
  - **Buffering and Retransmission**
  - **Error Concealment**
  - **Optional high quality audio compression**

External system

- **Seamless connection and control of selected TI audio codecs, DACs/ADCs and digital audio amplifiers using I2S and I2C**
- **HID functions like power control, binding, volume control, audio channel selection can be mapped to I/Os**
- **RoHS compliant 6mm x 6mm QFN-40 package**

RF section

- **5 Mbps over-the-air data rate**
- **Bandwidth-efficient modulation format**
- **Excellent link budget with programmable output power up to +3.5 dBm and -83 dBm sensitivity**
- **Seamless support for CC2590 range extender (+11dBm output power, -86dBm sensitivity)**
- **Suited for systems targeting compliance with worldwide radio frequency regulations: ETSI EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)**

Digital audio support

- **Digital I2S audio interface supports 1 or 2 audio channels at sample rates of 32, 40.275, 44.1 and 48 kHz, and supports 16 bit word-widths**
- **Audio latency down to 20 ms**
- **Data side-channel allows data to be sent alongside the audio between external host controllers**

Development tools

- **PC-based PurePath™ Wireless Configurator (PPW Configurator) for CC8520 configuration**
- **CC8520 User's Guide**
- **CC85XXDK audio development kit**
- **No software development needed**

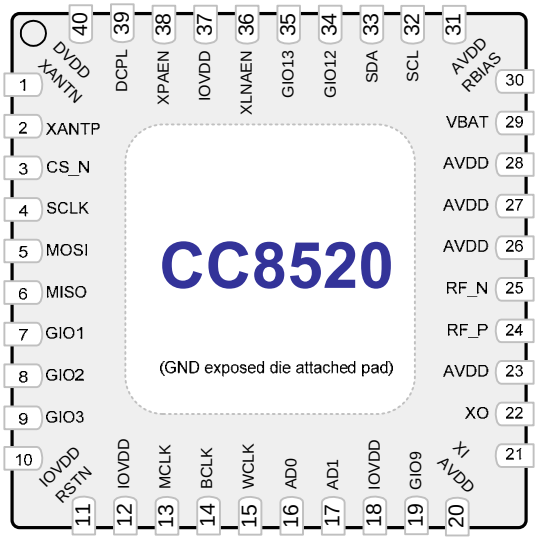
DESCRIPTION

The PurePath™ Wireless platform is a cost-effective and low-power solution optimized for wireless transmission of high-quality digital audio.

The CC8520 includes a robust built-in wireless audio transmission protocol and can control selected external audio devices. Utilizing numerous coexistence mechanisms allows the CC8520 to avoid interfering with, or being interfered by other 2.4 GHz radio systems. The CC8520, which supports 2 audio channels, is the first device in the PurePath™ Wireless platform.

The CC8520 operates autonomously, and can be used with or without an external MCU. An external host processor can be connected through SPI and control some aspects of its operation. The CC8520 interfaces easily with other TI audio ICs and DSPs (using I2S and DSP/TDM interfaces).

QFN-40 PACKAGE (TOP VIEW)



ABBREVIATIONS

ADC	Analog to Digital Converter	LAN	Local Area Network
ARIB	Association of Radio Industries and Businesses	LED	Light Emitting Diode
BER	Bit Error Rate	LNA	Low Noise Amplifier
CODEC	Coder/Decoder	MISO	Master In Slave Out
DAC	Digital to Analog Converter	MOSI	Master Out Slave In
DRC	Dynamic Range Control	MCU	Microcontroller
DSP	Digital Signal Processor	PA	Power Amplifier
EHIF	External Host Interface	PCM	Pulse Code Modulation
ESD	Electro Static Discharge	PER	Packet Error Rate
ETSI	European Telecommunications Standard Institute	PLL	Phase Lock Loop
FCC	Federal Communications Commission	PM	Protocol Master
FEC	Forward Error Correction	PPW	PurePath™ Wireless
FSK	Frequency Shift Keying	PS	Protocol Slave
FW	Firmware	PWM	Pulse Width Modulation
HID	Human Interface Device	RoHS	Restriction of Hazardous Substances
I2C	Inter-Integrated Circuit (serial communications bus)	RF	Radio Frequency
I2S	Inter-IC Sound (serial bus for digital audio signals)	SPI	Serial Peripheral Interface
IEEE	Institute of Electrical and Electronics Engineers	SoC	System-on-Chip
ISM	Industrial, Scientific, Medical	STD	Standard
JEDEC	Joint Electron Device Engineering Council	TDM	Time-Division Multiplexing

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	TEST CONDITIONS	Min	Max	Unit
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	min(VDD + 0.3, 3.9)	V
Input RF level			10	dBm
Storage temperature range		-40	85	°C
Reflow soldering temperature	According to IPC/JEDEC J-STD-020		260	°C
ESD (2)	All pads, according to human-body model (HBM), JEDEC STD 22, method A114		2000	V
	According to charged-device model (CDM), JEDEC STD 22, method C101E		400	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) CAUTION: ESD sensitive device. Precaution should be used when handing the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	Min	Max	Unit
Operating ambient temperature range, T_A		-40	+85	°C
Operating supply voltage		2.0	3.6	V

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC8520 EM reference designs with T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RF frequency range		2400		2483.5	MHz
Data rate	Shaped 8FSK		5		Mbps
Current consumption, power down state	Voltage regulator / crystal oscillator off – status lost (POWERED_DOWN state)		1		µA
Current consumption, audio sink	Average current for audio sink with I2S interface active and uncompressed stereo audio link at 48 kHz, 16 bits. (PCM16)		25		mA
Current consumption, audio source	Average current for audio source with I2S interface active and uncompressed stereo audio link at 48 kHz, 16 bits, maximum output power. (PCM16)		29		mA
Audio latency	Latency between I2S interface on audio source and I2S interface on audio sink. Uncompressed 16 bit. Audio latency is programmable using the PPW Configurator [1].	768		2048	Samples
Audio sample rate	Audio sample rate is programmable using the PPW Configurator [1] (1)		48 44.1 40.275 32		kHz

(1) ±2000ppm tolerance

RF CHARACTERISTICS, CC8520

Measured on Texas Instruments CC8520 EM reference designs with T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Output power	Maximum output power setting		3.5		dBm
Receiver sensitivity	5 Mbps, 0.1 % BER		-83		dBm
Saturation (maximum input level)	5 Mbps, 0.1 % BER		-2		dBm
Selectivity	Adjacent channel, ±4MHz, wanted 3dB above sensitivity		8		dB
	Alternate channel, ±8MHz, wanted 3dB above sensitivity		35		dB
Occupied bandwidth	99% energy bandwidth		3.8		MHz
Spurious emission	Suitable for systems targeting compliance with EN 300 328, EN 300 440(1), FCC CFR47 Part 15 and ARIB STD-T-66				

(1) Systems with external antenna connector: Margins for passing conducted requirements at sub 1GHz frequencies can be improved by using a simple band-pass filter connected between matching network and RF connector (1.6 pF in parallel with 1.6 nH); this filter must be connected to a good RF ground.

48-MHz CRYSTAL REQUIREMENTS

General parameters with T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Crystal frequency			48		MHz
Crystal frequency accuracy requirement(1)		-50		50	ppm
ESR Equivalent series resistance		-		60	ohm
C_0 Crystal shunt capacitance		-		3	pF
C_L Crystal load capacitance		15	16	17	pF

(1) Including aging and temperature dependency

AUDIO PLL CHARACTERISTICS

T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
MCLK Frequency range	Programmable using the PPW Configurator [1]	$32 \cdot F_{WCLK}$		$512 \cdot F_{WCLK}$	
BCLK Frequency range	Programmable using the PPW Configurator [1]	$32 \cdot F_{WCLK}$		$256 \cdot F_{WCLK}$	
WCLK Frequency range		31.936		48.096	kHz
RMS jitter	RMS period jitter for 1000 periods		80	200	ps

1 PIN DESCRIPTION

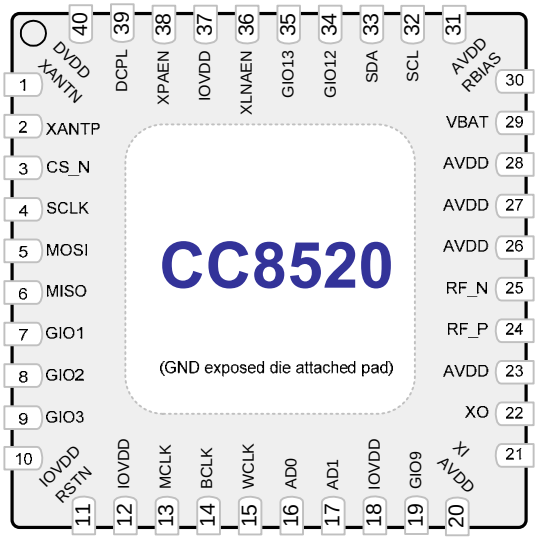


Figure 1 - CC8520 QFN Package Top View

PIN	PIN NAME	PIN TYPE	DESCRIPTION
-	GND	Ground	The exposed die attach pad must be connected to a solid ground plane underneath the chip
1	XANTN	Digital I/O[1]	FW2.0: Controlling external antenna switch (FW1.0/FW1.1: NC)
2	XANTP	Digital I/O[1]	FW2.0: Controlling external antenna switch (FW1.0/FW1.1: NC)
3	CS_N	Digital Input (pull-up)	Serial SPI configuration interface, active low chip select
4	SCLK	Digital I/O[1]	Serial SPI configuration interface, clock input/output
5	MOSI	Digital I/O[1]	Serial SPI configuration interface, master data input, slave data output
6	MISO GIO0	Digital I/O[1]	Serial SPI configuration interface, master data output, slave data input GIO0 output when CS_N is deasserted. General-purpose digital I/O pin 0
7	GIO1	Digital I/O[1]	General-purpose digital I/O pin 1 Configurable with PurePath™ Wireless Configurator
8	GIO2	Digital I/O[1]	General-purpose digital I/O pin 2
9	GIO3	Digital I/O[2]	General-purpose digital I/O pin 3 Configurable with PurePath™ Wireless Configurator

PIN	PIN NAME	PIN TYPE	DESCRIPTION
10	IODVDD	Power (I/O pads)	Digital power supply for the digital I/Os in the SPI interface and GIO1-GIO3.
11	RSTN	Digital Input (pull-up)	Active-low device reset
12	IOVDD	Power (I/O pins)	Digital power supply for the RSTN and MCLK digital I/O pins.
13	MCLK GIO4	Digital I/O[1]	Master clock output for external audio devices General-purpose digital I/O pin 4
14	BCLK GIO5	Digital I/O[1]	I2S/DSP audio interface bit clock (in/out) General-purpose digital I/O pin 5
15	WCLK GIO6	Digital I/O[1]	I2S/DSP audio interface word clock (in/out) General-purpose digital I/O pin 6
16	AD0 GIO7	Digital I/O[1]	I2S/DSP audio interface data line 0 (in/out) General-purpose digital I/O pin 7
17	AD1 GIO8	Digital I/O[1]	I2S/DSP audio interface data line 1 (in/out) General-purpose digital I/O pin 8
18	IOVDD	Power (I/O pins)	Digital power supply for the digital I/Os in audio interface (BCLK-AD2).
19	AD2 GIO9	Digital I/O[2]	I2S/DSP audio interface data line 2 (in/out) Configurable with PurePath™ Wireless Configurator
20	AVDD	Power (Analog)	2.0-3.6V analog power supply connection
21	XI	Analog I/O	Crystal oscillator pin input, or external clock input (48 MHz)
22	XO	Analog I/O	Crystal oscillator pin output (48 MHz)
23	AVDD	Power (Analog)	Analog power supply connection
24	RF_P	RF I/O	Positive differential RF input signal to LNA in receive mode Positive differential RF output signal from PA in transmit mode
25	RF_N	RF I/O	Negative differential RF input signal to LNA in receive mode Negative differential RF output signal from PA in transmit mode
26	AVDD	Power (Analog)	Analog power supply connection
27	AVDD	Power (Analog)	Analog power supply connection
28	AVDD	Power (Analog)	Analog power supply connection
29	VBAT	Analog input	Battery voltage supervisor (threshold level programmable by external resistor to positive battery terminal)
30	RBIAS	Analog output	External precision bias resistor for reference current. 56 kΩ, ±1%
31	AVDD	Power (Analog)	Analog power supply connection (Guard ring AVDD connection for digital noise isolation)
32	SCL GIO10	Digital I/O[1]	I2C master clock line. Must be connected to external pull-up General-purpose digital I/O pin 10
33	SDA GIO11	Digital I/O[1]	I2C master data line. Must be connected to external pull-up General-purpose digital I/O pin 11
34	GIO12	Digital I/O[1]	General-purpose digital I/O pin 12
35	GIO13	Digital I/O[1]	General-purpose digital I/O pin 13
36	XLNAEN	Digital I/O[2]	Control external LNA
37	IODVDD	Power (I/O pads)	Digital power supply for SCL-GIO15 pins.
38	XPAEN	Digital I/O[2]	Control external PA

PIN	PIN NAME	PIN TYPE	DESCRIPTION
39	DCPL	Power (Digital)	1.7V-1.85 V linear voltage regulator output to which a 1 uF decoupling capacitor should be attached. For test-purposes an external digital supply voltage (1.62-1.98 V) can be applied here, bypassing the voltage regulator. NOTE: The voltage regulator is intended for use with the CC8520 chip only. It cannot be used to provide supply voltage to other devices.
40	DVDD	Power (Digital)	Digital power supply for the linear voltage regulator.

[1] Digital I/O pad with 4 mA source/sink capability, programmable direction and pull-up, pull-down or high-impedance.
[2] Digital I/O pad with 20 mA source/sink capability, programmable direction and pull-up, pull-down or high-impedance.

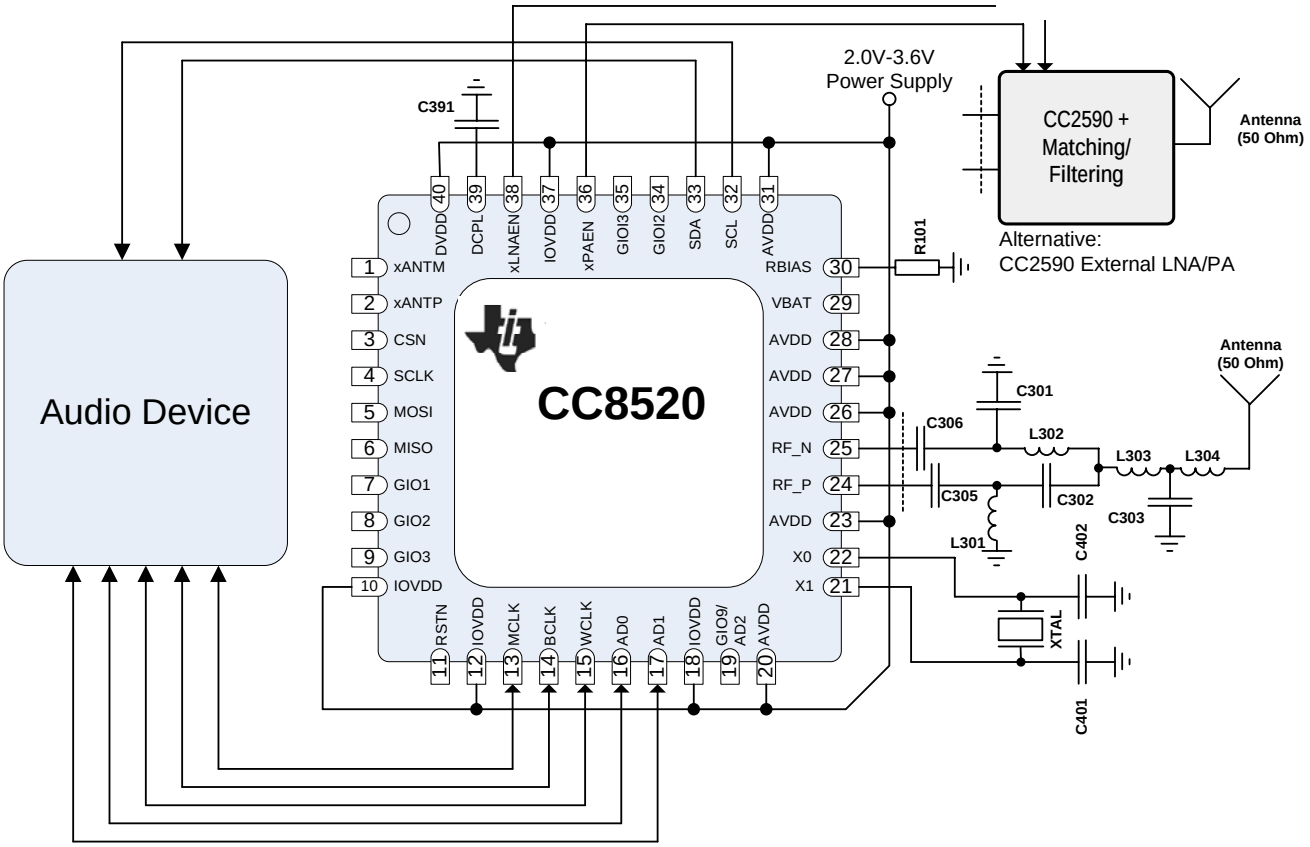


Figure 2 - CC8520 Application Circuit

2 SYSTEM DESCRIPTION

The CC8520 is a 2.4GHz wireless SoC operating in the 2.4 GHz ISM band designed for streaming digital audio wirelessly. It is designated to operate autonomously (without any host MCU) but certain aspects of operation can be controlled by a host MCU.

Before operation, the CC8520 must be programmed with a user-specific FW image, which can be created using the PPW Configurator [1]. The configuration file can be programmed into the on-chip Flash memory by using the PPW Configurator and the CC Debugger [2] and is also programmable in a production line. The configuration image contains information identifying the device as a master or a slave, how many channels are supported, the direction of the audio channels, HID support, audio device supported and more.

If CC8520 is configured as a slave, it will automatically start searching for a valid audio network. If configured as a master, it will start a new network. As soon as a network is formed, audio transmission will commence.

The CC8520 will automatically configure an attached supported audio IC (see compatibility list for a list of supported ICs in chapter 3).

3 SUPPORTED AUDIO DEVICES

Supported ADC/DAC/Codec/Amplifier Devices

The following device drivers will initially be implemented:

Device	DESCRIPTION
AIC3101	Low-Power Stereo Codec with 6 Inputs, 6 Outputs, Speaker/HP Amp and Enhanced Digital Effects
AIC3104	Low-Power Stereo CODEC with 6 Inputs, 6 Outputs, HP Amp and Enhanced Digital Effects
ADC3101	92dB SNR Low-Power Stereo ADC with Digital Mic Support
AIC3204	AIC3204: Very Low-Power Stereo Audio CODEC with Power Tune™ Technology

Note: The complete list of supported devices can be found in the PPW Configurator [1].

Supported SPDIF-RX / SPDIF-TX / DSP Devices

The following device drivers will be implemented:

Device	DESCRIPTION
DIR9001	96 kHz, 24-Bit Digital Audio Interface Receiver
DIT4096	96 kHz, Digital Audio Transmitter
DSP	Generic Digital Audio Device

Note: The complete list of supported devices can be found in the PPW Configurator [1].

Other audio devices

The CC8520 is compatible with any I2S-based audio device that does not need to be configured at power-up and that is compatible with the requirements listed in the audio interface (Chapter 6). It is also compatible with a wide range of TI DSPs using an I2S interface.

4 NETWORK TOPOLOGY AND NOMENCLATURE

A **CC8520 network** consists of one **Protocol Master** (PM) and one or two **Protocol Slave(s)** (PS). The PM provides the audio reference clock and controls network association. The PS regenerate the audio reference clock based on the packets received. Audio can be transmitted from the PM to a PS. The device receiving the audio is called an **Audio Sink**, the device sending the audio is called an **Audio Source**. A device can be both Audio Sink and Audio Source at the same time (bidirectional audio will be supported in future revisions of the firmware). The CC8520 network also includes a Data Side-Channel which is a bi-directional data link between the PM and all PS in the network. This is further described in chapter 8.

Figure 3 illustrates the different network topologies that can be formed with CC8520 using the different firmware versions.

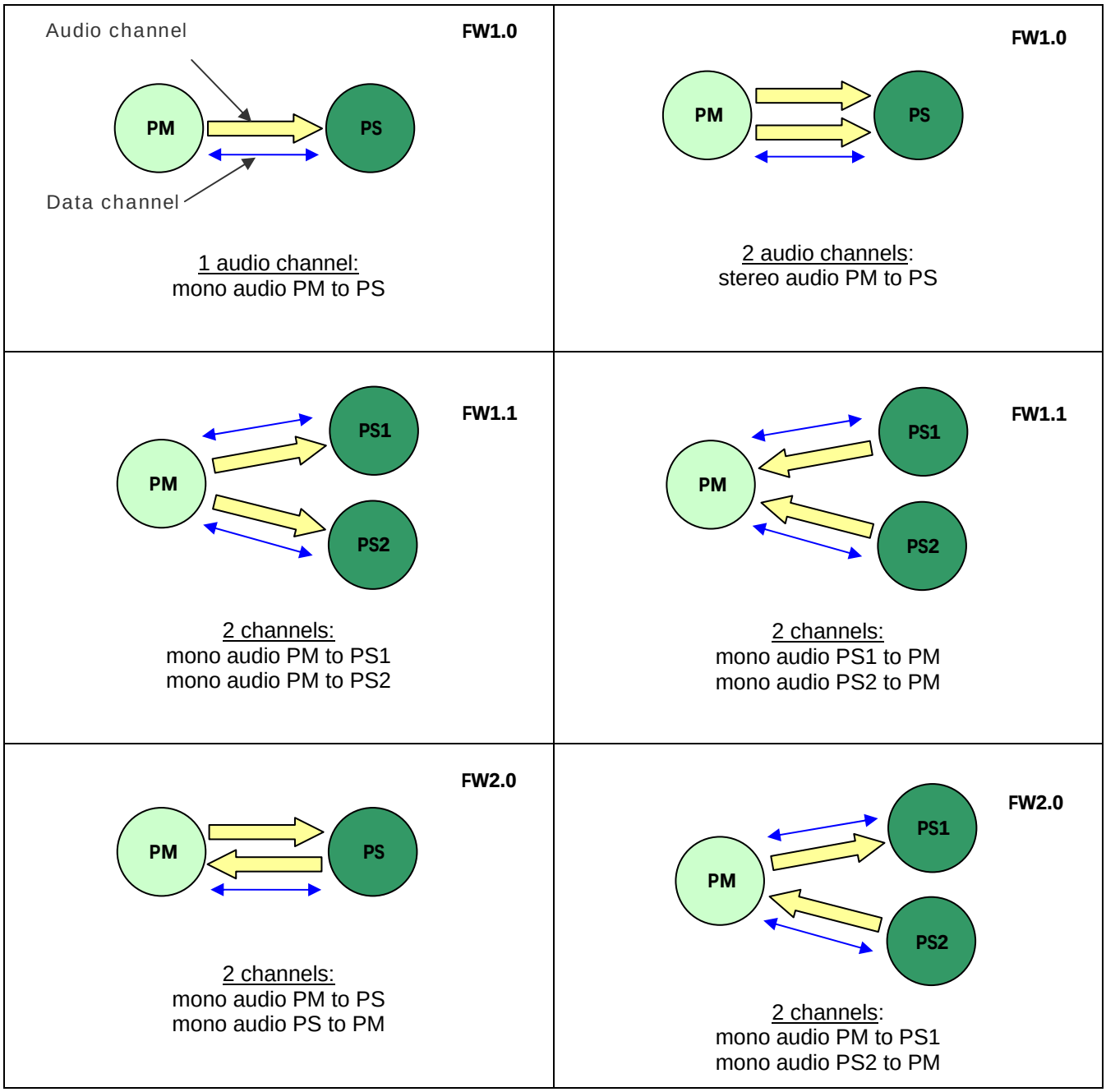


Figure 3 CC8520 topologies supported for different CC8520 FW revisions
(Yellow arrow = audio channel. Blue arrow = data side channel. PM = Protocol Master. PS = Protocol Slave)

5 COEXISTENCE AND AUDIO COMPRESSION

The CC8520 implements a wide range of techniques to maximize coexistence performance when operating in an environment with other 2.4 GHz wireless devices. The built-in protocol implements adaptive frequency hopping. This helps improve coexistence with RF sources that do not move around in frequency, such as IEEE 802.11 (Wireless LAN) devices, as well as providing robust performance in a multipath RF environment. Audio is buffered in the receiver, and any data which is not correctly received, is retransmitted utilizing the high raw datarate (5Mbps). When link quality is poor (e.g. when moving out of range), audio is muted until a reliable link is restored.

Forward Error Correction (FEC) is built into the CC8520 modulation scheme. Furthermore, packets are divided into independent sections so that an error in one section does not mean the whole packet is lost.

The CC8520 supports uncompressed PCM16 audio, with no modifications made to the digital audio. High quality audio compression can optionally be enabled and effectively reducing average current consumption by lowering the radio duty-cycle. Compression improves robustness further, as there is less data sent and more time available for retransmission.

6 AUDIO INTERFACE

The CC8520 audio interface is I2S compatible and it supports up to 2 audio channels. The audio interface on the protocol master can be configured as clock master (supplied from the internal audio PLL) or as clock slave (clock supplied from external audio IC).

The audio interface has 2 data pins. Each of these can be configured as an input, output or unused. The audio interface can be configured to support I2S. The CC8520 supports word widths of 16 to 24 bits, but over-the-air 16 bits is always used.

7 HUMAN INTERACTION DRIVERS (HID)

The CC8520 supports basic HID functionality without an external MCU. This means that some basic functionality can be controlled on the slave remotely from the master. The HID functionality supported includes:

- power control (to turn devices on/off)
- network binding (to pair devices)
- volume control (volume control can be managed locally)
- Status LED (blinking diode to indicate the status of the RF link)

All HID functions are configurable in the PPW Configurator [1] and can be mapped to the CC8520 I/O pins.

8 EXTERNAL HOST INTERFACE (EHIF / Data side channel)

The external host interface (EHIF) allows an external host device, e.g. a microcontroller, to:

- Control the operation of and poll status from the CC8520, mainly by taking over driver functionality.
- Communicate with other external host devices through an integrated data side-channel
- Get access to test functionality for audio, I/O and RF.

The external host interface is available via SPI with a single interrupt pin. The external host will act as SPI master and CC8520 will act as SPI slave.

User specified data can be transferred between the master EHIF and the slave EHIFs, in both directions using the data side-channel. The data side-channel establishes robust, ensured-delivery connections in both directions from any slave to the master or from master to any slave (direct slave to slave communication is not

available). There is no specified minimum throughput for the data side-channel but under normal operating conditions and data rate of up to 30 kbps is possible in each direction.

More details can be found in the CC8520 User's Guide [2].

9 REFERENCES

[1] PurePath™ Wireless Configurator

[2] CC8520 product folder

[3] CC-Debugger

PACKAGING INFORMATION

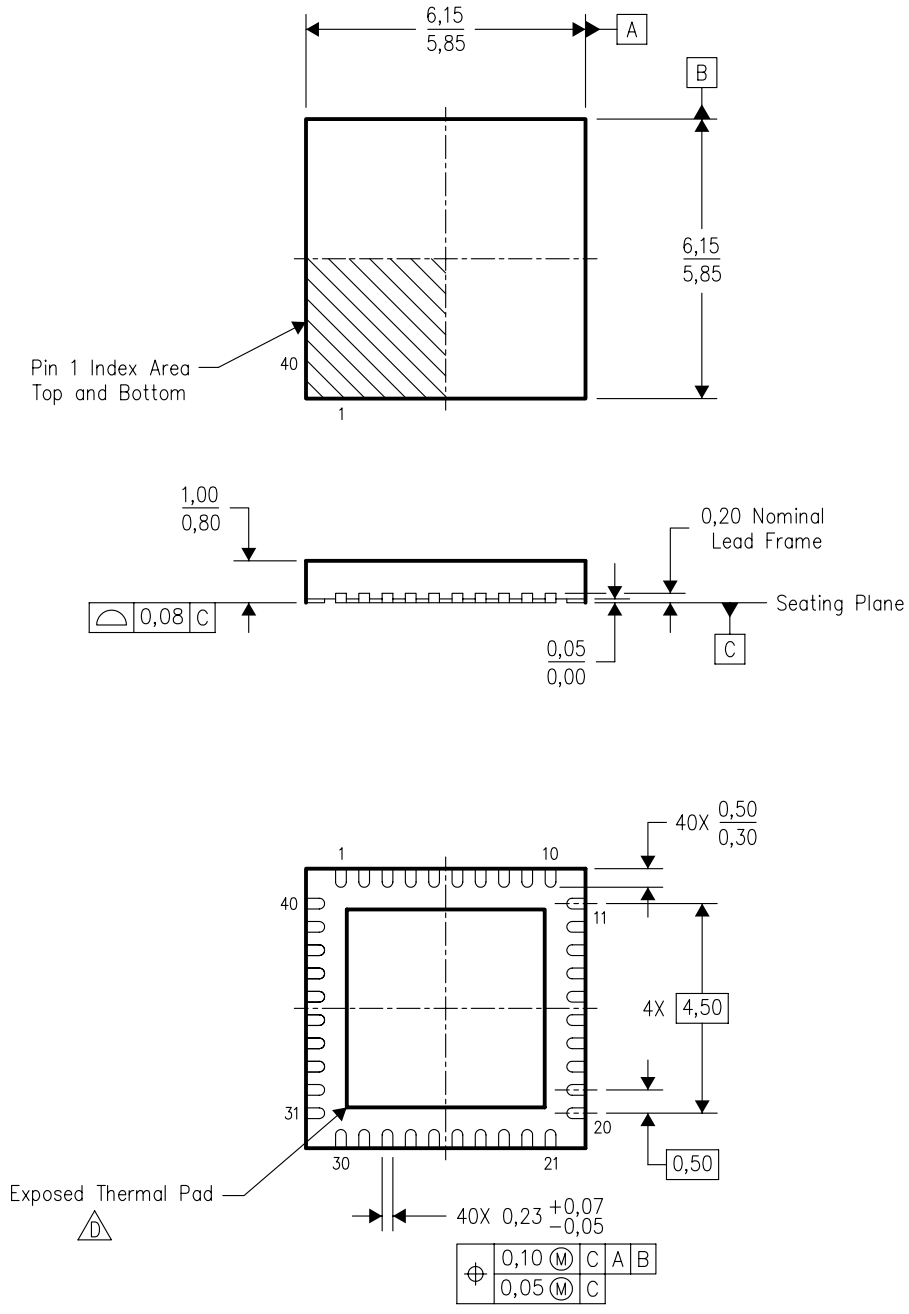
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CC8520RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CC8520RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RHA (S–PQFP–N40) PLASTIC QUAD FLATPACK



Bottom View

4204276/C 12/2004

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation VJJD–2.

THERMAL PAD MECHANICAL DATA

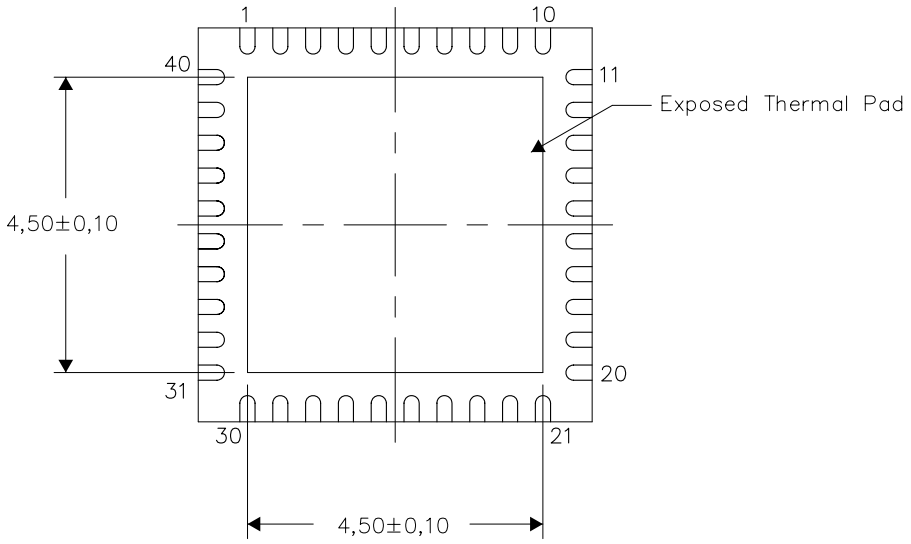
RHA (S–PVQFN–N40)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

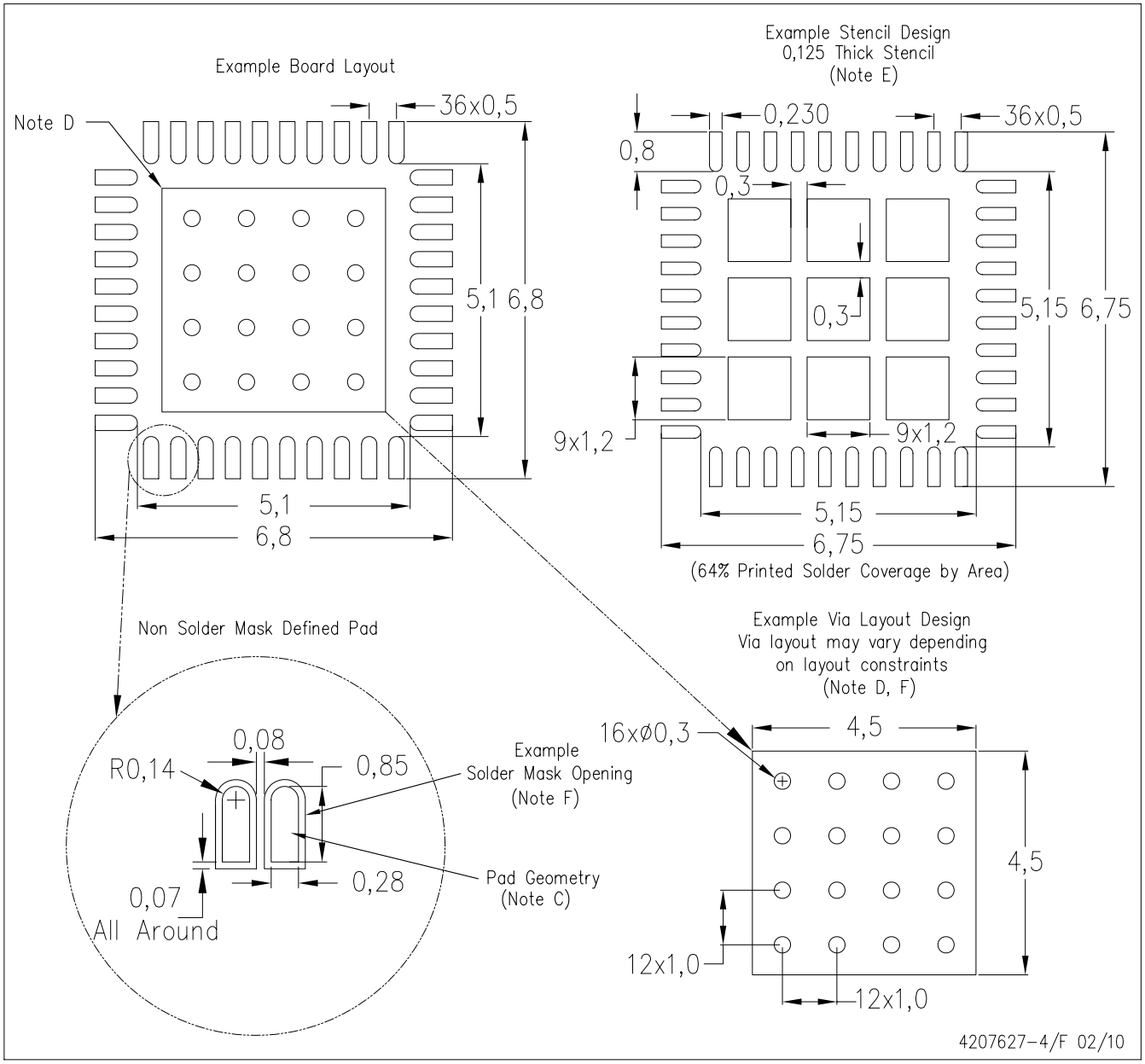


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHA (S–PVQFN–N40)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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